Abstract of the Disclosure

A 3-D graphics chip includes independent internal DRAM buffers each having a wide bandwidth access bus for connection to a 3-D texture rendering drawing engine. The 3-D drawing engine takes advantage of a flexible embedded memory interface to reduce the traditional 3-D pipeline delay by a factor of 3. In a specific embodiment, each of three drawing processes—texture, Z, pixel—retrieves and stores information in a separate embedded drawing buffer via separate wide bandwidth access busses. Access to an external memory is provided via a separate external access bus. In another specific embodiment, the 3-D drawing engine accesses the embedded drawing buffers via read and write FIFO's to maximize the drawing process throughput.